

2-party Secure Computation

Malicious Adversaries

Bar-Ilan Winter School, Feb 2015

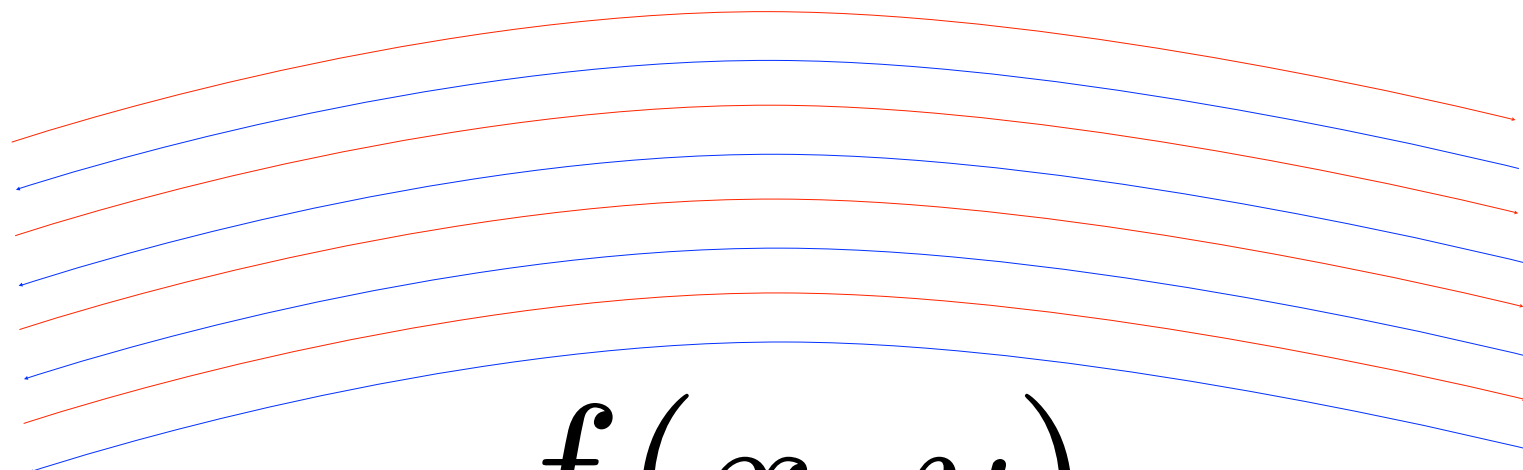
abhi shelat



Brief Survey



x



y

“...and nothing else”

The age of optimism

80s

90s

00s

10s

20s

PKE
SFE

PKE

PKE

Invented

Practical

Ubiquit

SFE

SFE

SFE

Feasible

Practical

Ubiquit

MNPS04
MNPS08
KS06, K08

Fairplay
Honest but curious

4k gates,
600 gates/sec

MNPS04

MNPS08

KS06, K08

LP04, LP07, LPS08

Fairplay

Honest but curious

4k gates,

600 gates/sec

Cut-and-choose

Malicious adv

1k gates,

4 gates/sec

2009

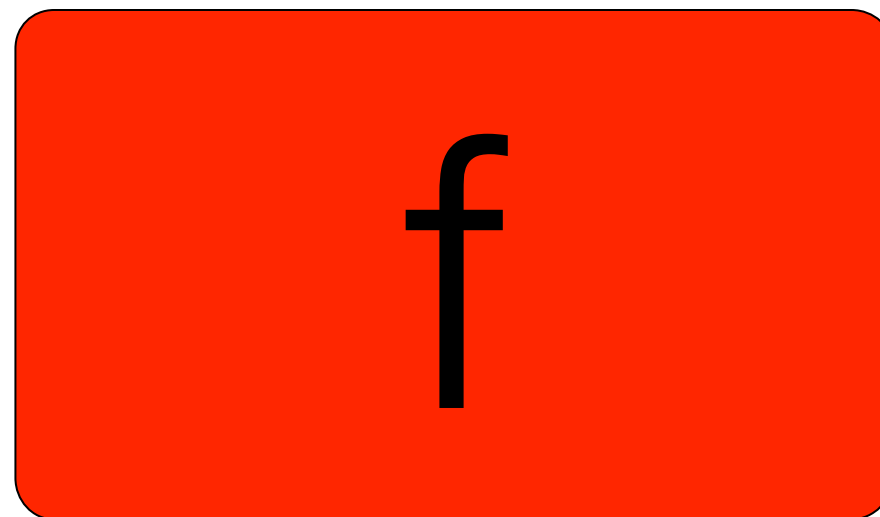
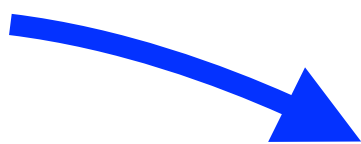
10x

PSSW09

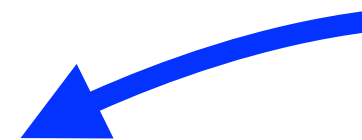
AES circuit
Malicious adv

40k gates,
35 gates/sec
(2^{-40} security)

Alice
x



Bob
y



$\text{AES}_x(y)$

MNPS04
MNPS08

KS06, K08

LP04, LP07, LPS08
PSSW09

LP10

JS07 JKS08

NO09

Fairplay
Honest but curious

Cut-and-choose
Malicious adv

Hybrid, C&C+ZK
Malicious adv

Yao + ZK
Malicious adv

Lego+
Malicious adv

4k gates,
600 gates/sec

1k gates,
4 gates/sec

MNPS04

MNPS08

KS06, K08

LP04, LP07, LPS08

PSSW09

LP10

JS07 JKS08

NO09

IPS08,09, LOP11

HL08, HL08b

Fairplay

Honest but curious

Cut-and-choose

Malicious adv

Hybrid, C&C+ZK

Malicious adv

Yao + ZK

Malicious adv

Lego+

Malicious adv

Better BB Cut-and-choose

Malicious adv

Tamper proof model

4k gates,

600 gates/sec

1k gates,

4 gates/sec

(2^{-40} security)

PSSW09

AES circuit

Malicious adv

40k gates,
35 gates/sec

SS11

Hybrid CC+ZK

Malicious adv

40k gates,
130 gates/sec

NNOB11

GMW + OT Ext

Malicious adv

40k gates,
20k gates/sec
(2^{-58} security) 3s/bloc

DPSZ11

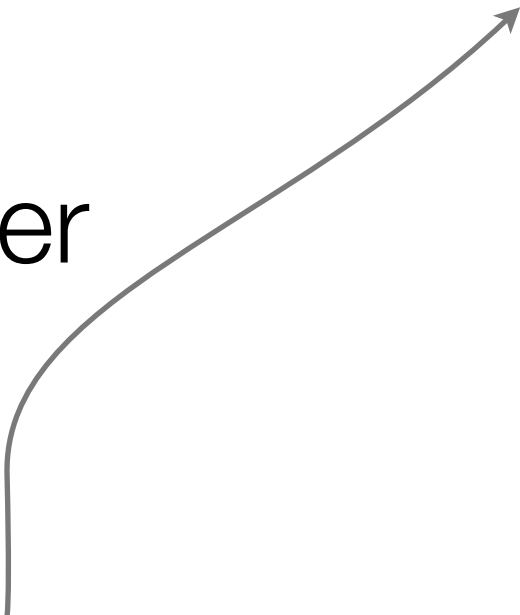
GMW + Beaver

Malicious adv

100k gates,
10 gates/sec
10ms/gate ~ 100 g/s

Amortized

5000x



2011

HEKM11

Pipeline + Circuit Lib

Honest but curious

40k gates

12k gates/sec

Bottleneck became the Compiler

2011

HEKM11

Pipeline + Circuit Lib

Honest but curious

40k gates

12k gates/sec

Bottleneck became the Compiler

JKS08

200x200 edit distance

660s

2011

HEKM11

Pipeline + Circuit Lib

Honest but curious

40k gates

12k gates/sec

Bottleneck became the Compiler

JKS08

200x200 edit distance

660s

HEKM11

1.2B nonxor gates

96k g/s

2k x 10k edit distance

2012

KSS12

1.2B nonxor gates	96k g/s
2k x 10k edit distance	
6B gates 4K x 4K edit distance	85k gates/sec
260m gate RSA-256	125k gates/sec
330m gate 2k x 2s Edit	123k gates/sec

MNPS04
MNPS08
KS06, K08
LP04, LP07, LPS08

PSSW09

LP11

SS11

KSS12

SS13

Fairplay
Honest but curious

Cut-and-choose
Malicious adv

AES circuit
Malicious adv

Hybrid, C&C+ZK
Malicious adv

Hybrid C&C+ZK
Malicious adv

Hybrid CC+ZK, Parallel
Malicious adv

CC, Parallel
Malicious adv

4k gates,
600 gates/sec

1k gates,
4 gates/sec

40k gates,
35 gates/sec

40k gates,
130 gates/sec

6B gates,
130k gates/sec

B gates,
1M gates/sec

More Garbled Circuits work

K08

Output Auth

KS08

Free XOR-trick

CKKZ12

Using circular 2-corr RHF

HEKM11

Pipeline + Circuit Lib
Honest but curious

40k- **1.2B** gates
12k-96k gates/sec

HS13

Less Memory, Parallel
Honest but curious

FN12

HMSG13

GPU system
Honest but curious

35M gates/se

Amortized

JS07 JKS08

Yao + ZK
Malicious adv

NO09

Lego+
Malicious adv

IPS08,09, LOP11

Better BB Cut-and-choose
Malicious adv

NNOB11

GMW + OT Ext
Malicious adv

DPSZ11

GMW + Beaver + SHE
Malicious adv 100k ops
10ms/"op" ~ 100 ops/s

DKLPSS12

500 ops/s

SZ13

GMW + OT Ext Fast
??

Advanced Techniques

Cut & choose

Lindell¹³

Huang-Evans-Katz¹³

Amortization: C&C + LEGO

Huang-Katz-Kolesnikov-Kumaresan-Malozemoff¹⁴

Lindell-Riva¹⁴

Garbling

Zahur-Evans-Rosulek¹⁴

Malkin-Pastro-shelat¹⁵

Algorithmic

Venkatasubramanian-shelat¹⁵

ORAM Secure Computation

Gordon-Katz-Kolesnikov-Krell-Malkin12

Keller-Scholl14

- 4 accesses/second to oblivious array of size one million
- Dijkstra's algorithm:
 - 2^{11} vertices and 2^{12} edges in 10 hours
 - 2^{18} vertices and 2^{19} edges in 14 months
(estimated from running a fully functional program)

Wang-Huang-Chan-shelat-Shi14

SCORAM: 4m gates/ORAM op

Wang-Chan-Shi14

CORAM: 500k gates/ORAM op

BenSasson-Chiesa-Tromer-Virza14

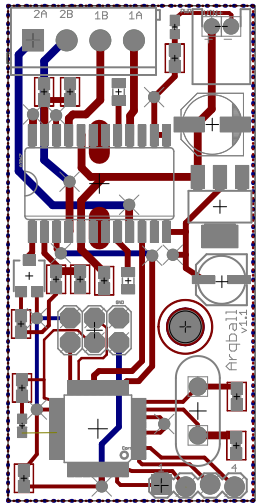
TinyRAM

Question: which secure
computation techniques
are preferable?

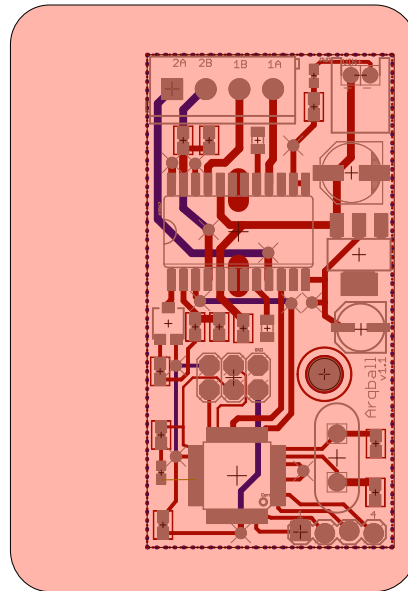
overhead

2-party Secure computation

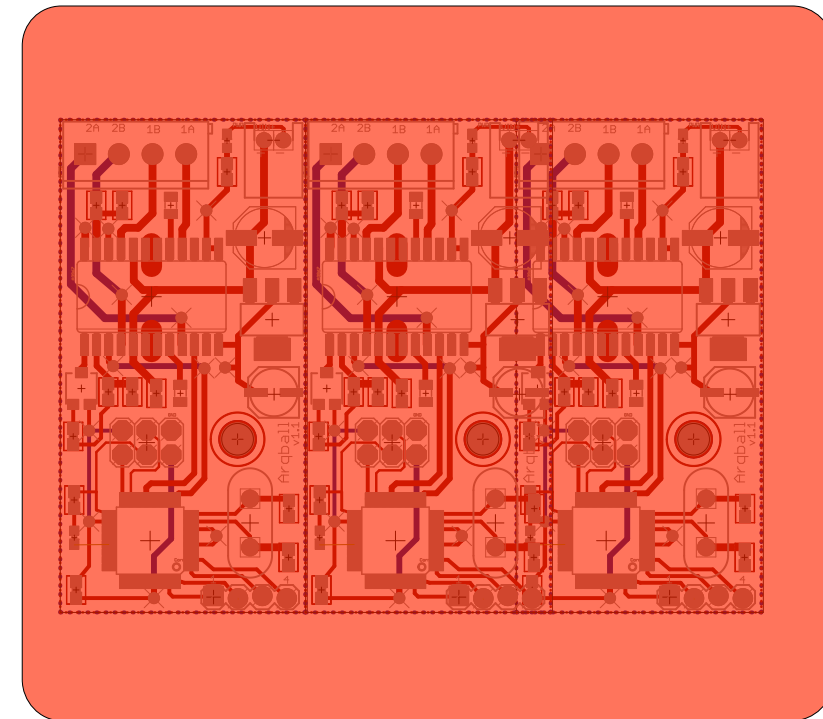
Plain



HBC



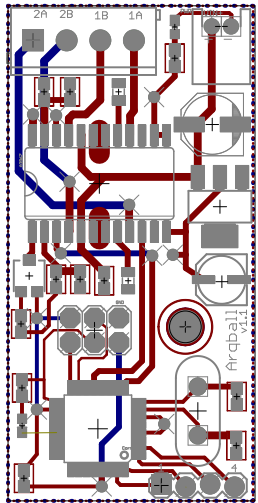
Malicious



overhead

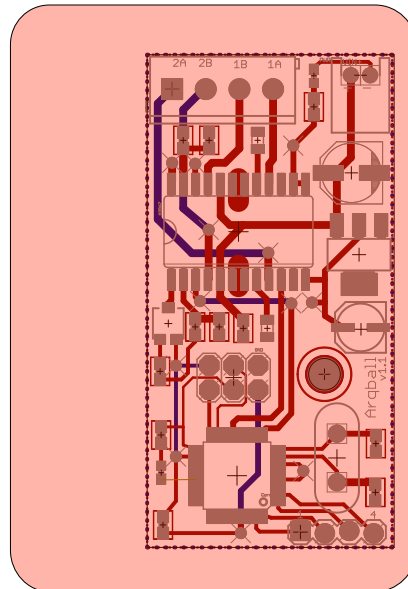
2-party Secure computation

Plain



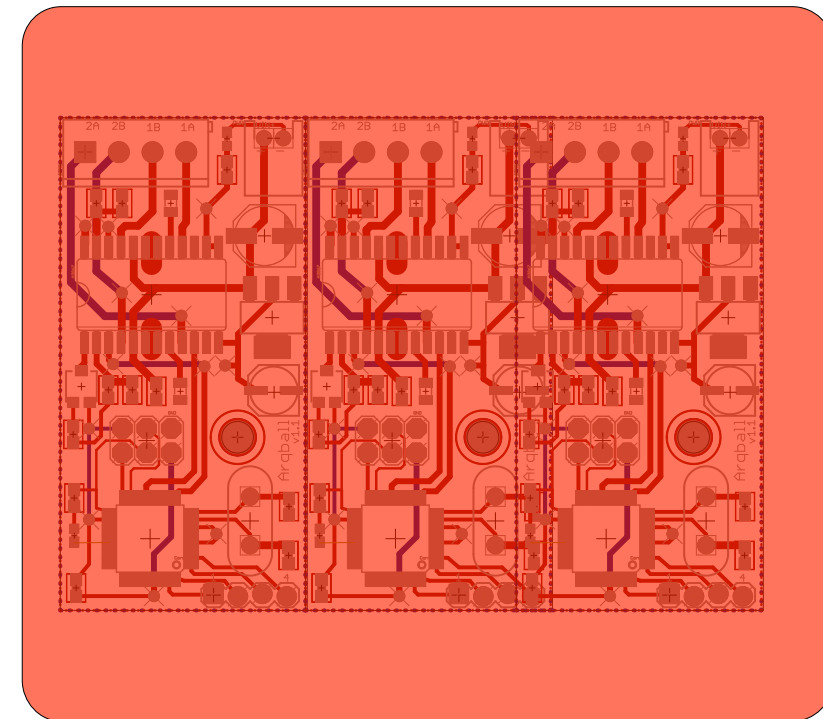
Comm
Comp
Assumption★

HBC



Comm
Comp
Assumption

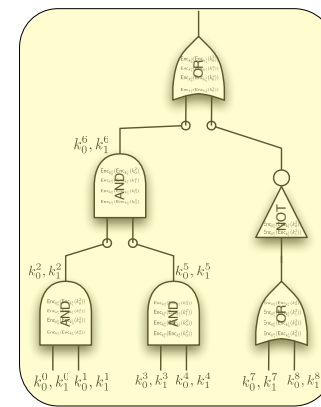
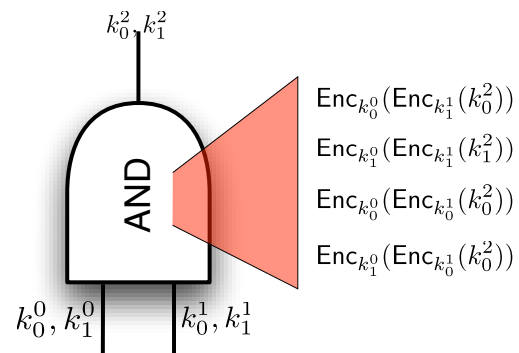
Malicious



Parallelizability is KEY

Garbled circuits

Y82



0 1 c

Oblivious
Transfer

Garbled gates + Composition + Key Mgmt

Honest-but-curious

$f(x,y)$



x



y

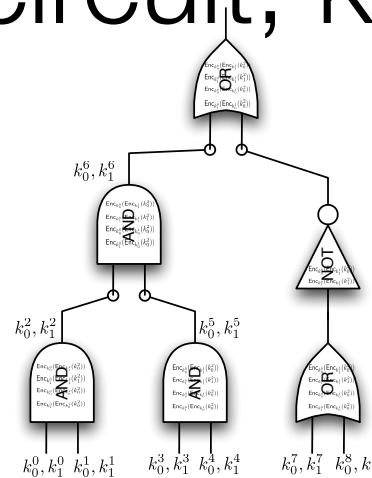
OT 1st msg



OT 2nd msg



Garbled circuit, keys for x



2 round!



1. Incrementally construct
maliciously-secure protocol

Definition

$$\forall A \exists S \forall (x_1, x_2), z$$

$$\mathbf{IDEAL}_{f,S(z),I}(x_1, x_2, k) \approx_c \mathbf{REAL}_{f,A(z),I}(x_1, x_2, k)$$

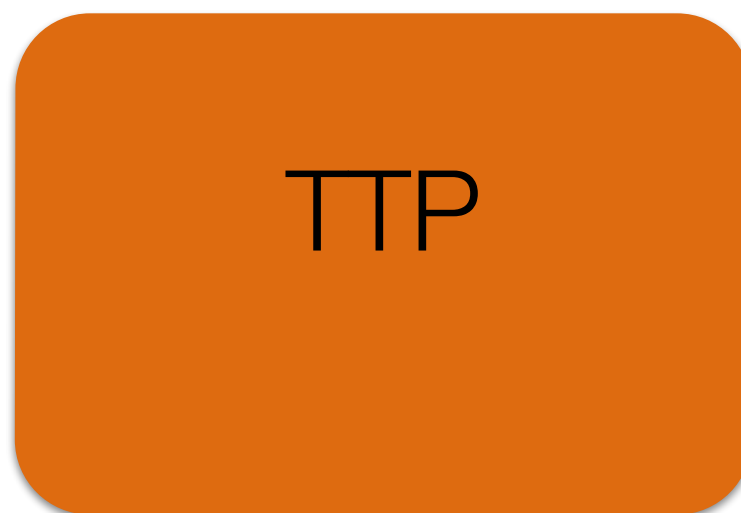
IDEAL_{S,I}



x



y



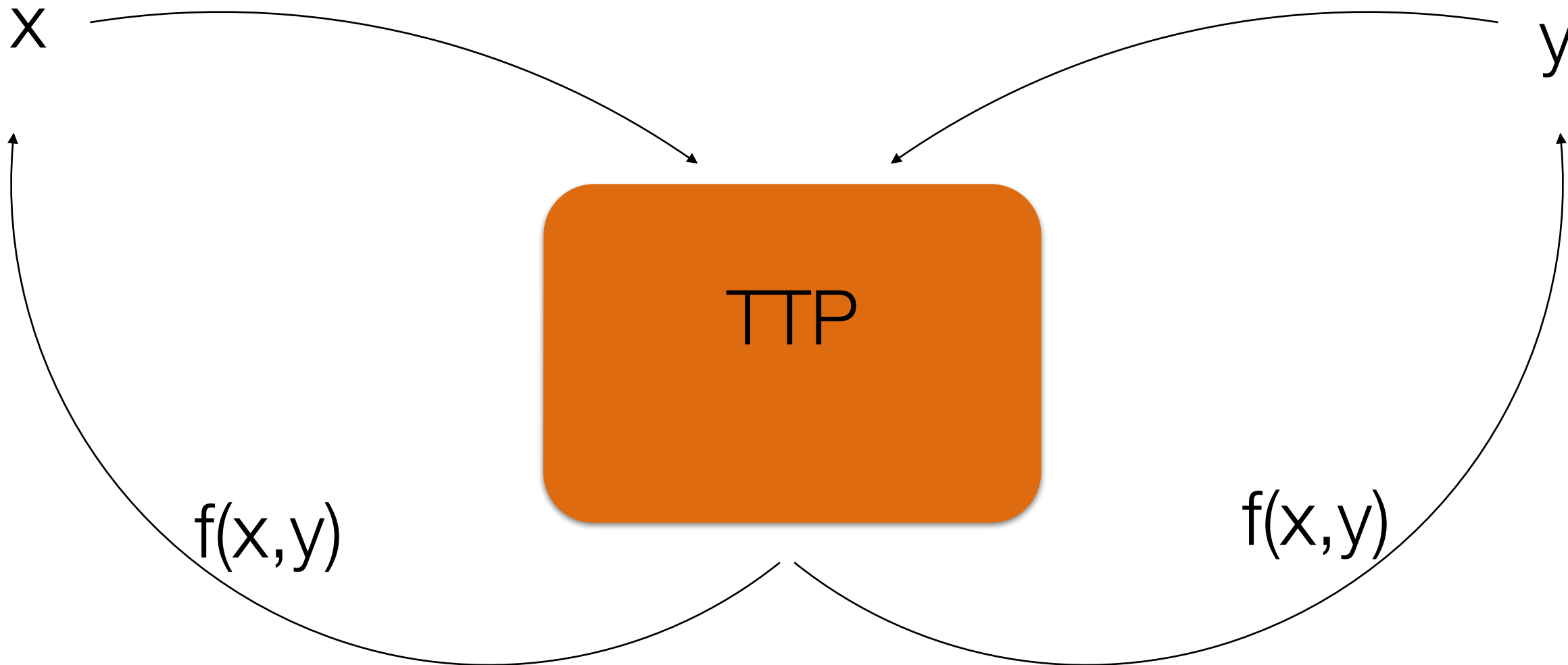
TTP

$f(x,y)$

$f(x,y)$

out: $f(x,y)$

out: $f(x,y)$



IDEAL_{S,I}



x



y

y'

abort?



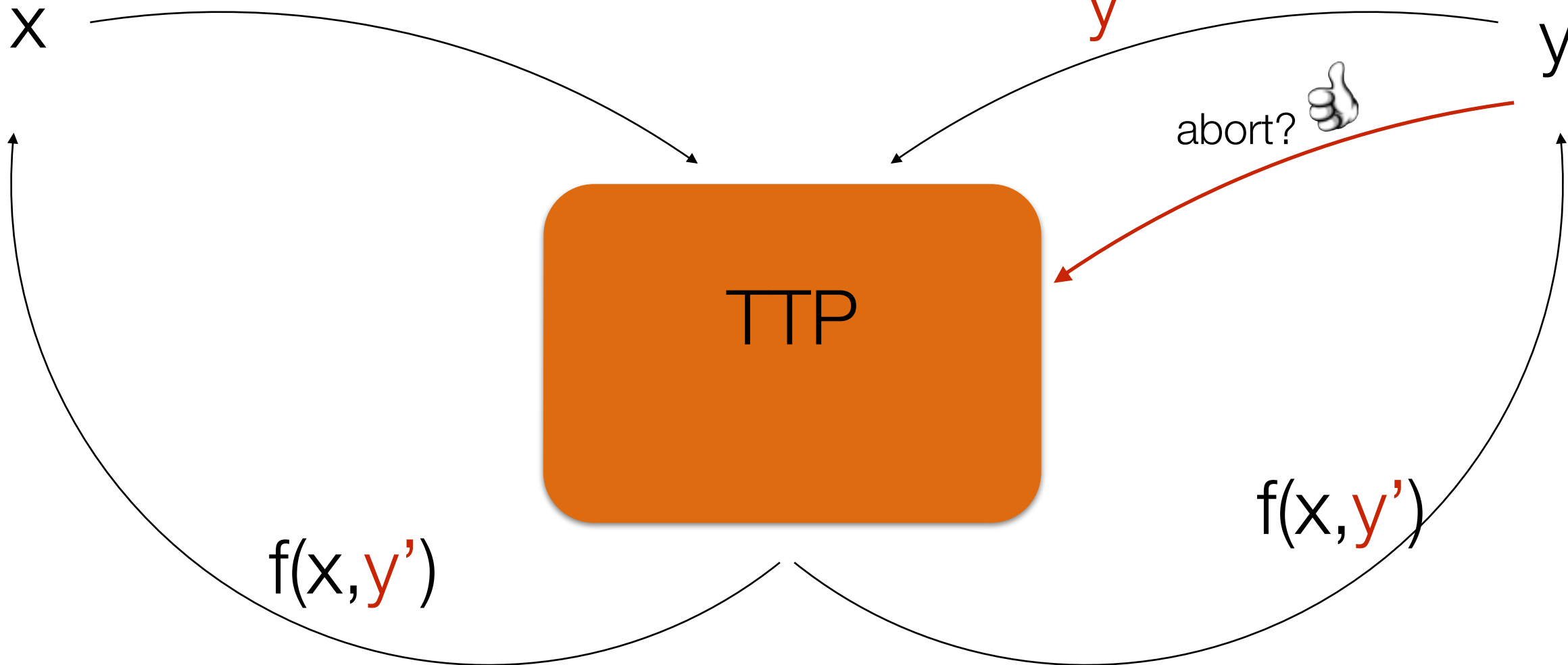
TTP

$f(x, y')$

$f(x, y')$

out: $f(x, y)$

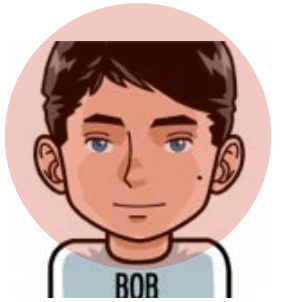
out:?



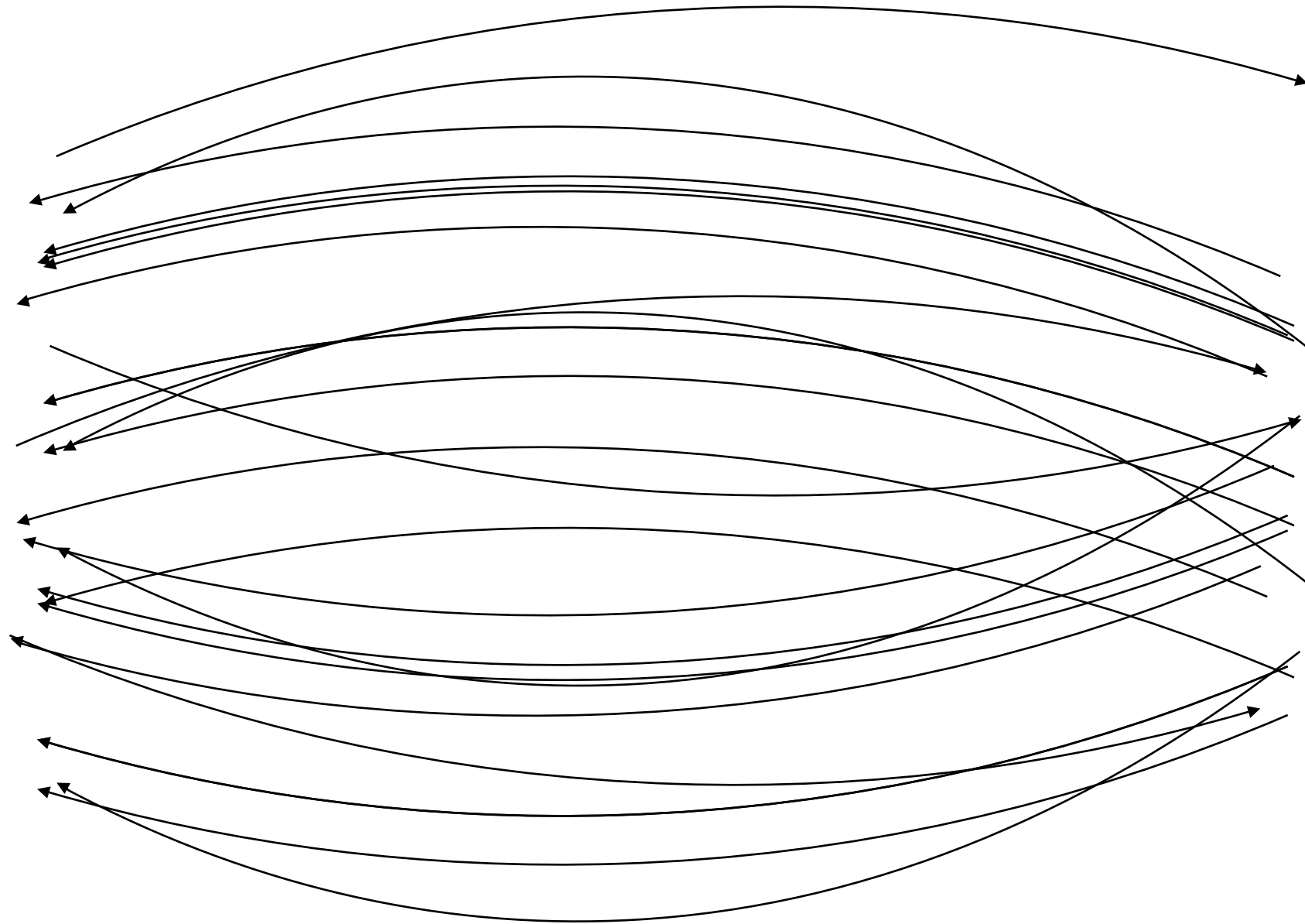
REAL_{A,I}



x



y



out:f(x,y)

out:?

Definition

$$\forall A \exists S \forall (x_1, x_2), z$$

$$\mathbf{IDEAL}_{f,S(z),I}(x_1, x_2, k) \approx_c \mathbf{REAL}_{f,A(z),I}(x_1, x_2, k)$$

1. Incrementally construct maliciously-secure protocol

2. Optimize

What can go wrong?



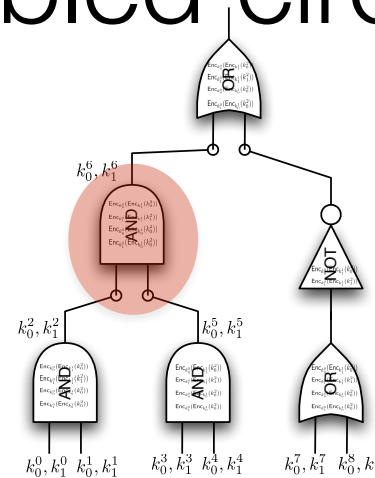
OT 1st msg



OT 2nd msg



Garbled circuit



sending a bad circuit

Prove circuit is good

GMW, Jarecki-Shmatikov07

$$\bigwedge_{g \in G} \text{CorrectGarble}_g \wedge \bigwedge_{w \in W} \text{GoodKeys}_w \wedge \bigwedge_{w \in W_S} \text{CorrectInput}_w \\ \wedge \bigwedge_{w \in W_R} \text{ZKS}_w \wedge \bigwedge_{w \in W_O} \text{CorrectOutput}_w$$

where

$$\begin{aligned} \text{GoodKeys}_w &= \text{ZKNotEq}(C_0^w, C_1^w) \\ \text{CorrectInput}_w &= (\text{ZKDL}(\mathbf{g}, C_0^w / \alpha^{x_{b_w}^w}) \wedge \text{ZKDL}(\mathbf{g}, C_b)) \vee \\ &\quad (\text{ZKDL}(\mathbf{g}, C_1^w / \alpha^{x_{b_w}^w}) \wedge \text{ZKDL}(\mathbf{g}, C_b / \alpha)), \text{ where } C_b \text{ is the} \\ &\quad \text{sCS commitment inside } \text{Com}_{cid_{S_i}} \text{ if } w \text{ is the } i^{th} \text{ input wire of } S \\ \text{CorrectOutput}_w &= \text{ZKPlainEq2}(E_0^w, C_0^w, 0) \wedge \text{ZKPlainEq2}(E_1^w, C_1^w, 1) \end{aligned}$$

$$\begin{aligned} \text{CorrectGarble}_g &= \text{CorrectShuffle}(0, 0) \vee \text{CorrectShuffle}(0, 1) \vee \\ &\quad \text{CorrectShuffle}(1, 0) \vee \text{CorrectShuffle}(1, 1) \end{aligned}$$

$$\begin{aligned} \text{CorrectShuffle}(\alpha, \beta) &= \text{CorrectCipher}(0, 0, \alpha, \beta) \wedge \text{CorrectCipher}(0, 1, \alpha, \beta) \wedge \\ &\quad \text{CorrectCipher}(1, 0, \alpha, \beta) \wedge \text{CorrectCipher}(1, 1, \alpha, \beta) \end{aligned}$$

$$\begin{aligned} \text{CorrectCipher}(\sigma_A, \sigma_B, \alpha, \beta) &= \text{ZKPlainEq}(F_{\alpha\beta}^{(1)}, C_{\alpha \oplus \sigma_A}^A, D_{\alpha\beta}) \wedge \\ &\quad \text{ZKPlainEq}(F_{\alpha\beta}^{(2)}, C_{\beta \oplus \sigma_B}^B, (C_{g(\alpha \oplus \sigma_A, \beta \oplus \sigma_B)}^C / D_{\alpha\beta})) \end{aligned}$$

$$\text{CorrectGarble}_g = \text{CorrectShuffle}(0, 0) \vee \text{CorrectShuffle}(0, 1) \vee \\ \text{CorrectShuffle}(1, 0) \vee \text{CorrectShuffle}(1, 1)$$

$$\text{CorrectShuffle}(\alpha, \beta) = \text{CorrectCipher}(0, 0, \alpha, \beta) \wedge \text{CorrectCipher}(0, 1, \alpha, \beta) \wedge \\ \text{CorrectCipher}(1, 0, \alpha, \beta) \wedge \text{CorrectCipher}(1, 1, \alpha, \beta)$$

$$\text{CorrectCipher}(\sigma_A, \sigma_B, \alpha, \beta) = \text{ZKPlainEq}(F_{\alpha\beta}^{(1)}, C_{\alpha \oplus \sigma_A}^A, D_{\alpha\beta}) \wedge \\ \text{ZKPlainEq}(F_{\alpha\beta}^{(2)}, C_{\beta \oplus \sigma_B}^B, (C_{g(\alpha \oplus \sigma_A, \beta \oplus \sigma_B)}^C / D_{\alpha\beta}))$$

32-clause Sigma-protocol PER gate

Given $\text{com}(K_x^0)$, $\text{com}(K_x^1)$, $\text{com}(K_y^0)$, $\text{com}(K_y^1)$, $\text{com}(K_w^0)$, and $\text{com}(K_w^1)$, P_2 needs P_1 to prove that the AND gate $(\delta, T_4, T_5, \sigma, T_\sigma)$ is correctly computed.

More specifically,

- (a) P_1 sends $\text{com}(\delta; r)$ to P_2 , and P_1 proves that $\text{com}(\delta; r) = q^\delta h^r$.
- (b) For every $(b_0, b_1) \in \{0, 1\}^2$, let $i = 2 * b_0 + b_1$, P_1 sends $\text{com}(T_i)$ to P_2 and proves that

$$\frac{\left(\text{com}(K_x^{b_0}) \text{com}(K_y^{b_1}) \text{com}(\delta) = \text{com}(K_x^{b_0} + K_y^{b_1} + \delta) \right) \wedge \left(\text{com}(T_i) = \text{com}(K_x^{b_0} + K_y^{b_1} + \delta)^{K_x^{b_0} + K_y^{b_1} + \delta} \right)}{}$$

Moreover, P_1 proves that $T_i \in \mathbb{Z}_N^*$ for $i = 0, 1, 2, 3$.

- (c) Let $\text{Mask}(b_0, b_1)$ denote the case that $(K_x^0)_N = b_0$ and $(K_y^0)_N = b_1$. P_1 proves to P_2 that

$$\text{mask}(0, 0) \vee \text{mask}(0, 1) \vee \text{mask}(1, 0) \vee \text{mask}(1, 1).$$

In particular, for case $\text{mask}(b_0, b_1)$, let

$$\begin{cases} a_0 = 2 \cdot b_0 + b_1 \\ a_1 = 2 \cdot b_0 + (1 - b_1) \end{cases} \quad \text{and} \quad \begin{cases} a_2 = 2 \cdot (1 - b_0) + b_1 \\ a_3 = 2 \cdot (1 - b_0) + (1 - b_1) \end{cases}.$$

It is defined that

$$\underline{\text{mask}(b_0, b_1)} = (P(\underline{a_0}) = \underline{T_0}) \wedge (P(\underline{a_1}) = \underline{T_1}) \wedge (P(\underline{a_2}) = \underline{T_2}) \wedge (Q(\underline{a_3}) = \underline{T_3}),$$

where $P(x)$ is the Lagrange polynomial coincides at points $(-1, K_w^0)$, $(4, T_4)$, $(5, T_5)$, and (σ, T_σ) ; and $Q(x)$ is the Lagrange polynomial coincides at points $(-1, K_w^1)$, $(4, T_4)$, $(5, T_5)$, and (σ, T_σ) .

Can optimize to ~19-clauses PER gate

Open problem to
optimize so as to
outperform C&C

Cut &
Choose

First Idea: Cut & Choose



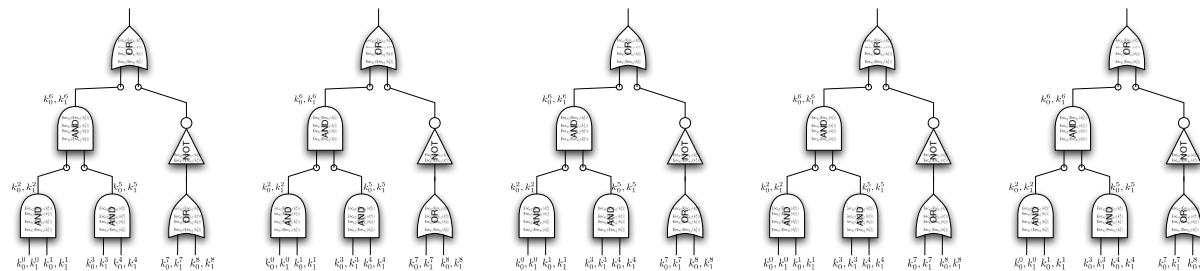
OT 1st msg



OT 2nd msg



Send **k** fresh garbled circuits



First Idea: Cut & Choose



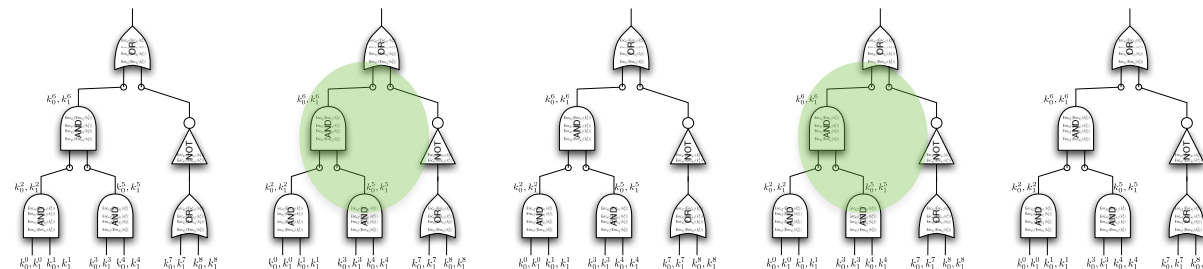
OT 1st msg



OT 2nd msg



Send **k** fresh garbled circuits

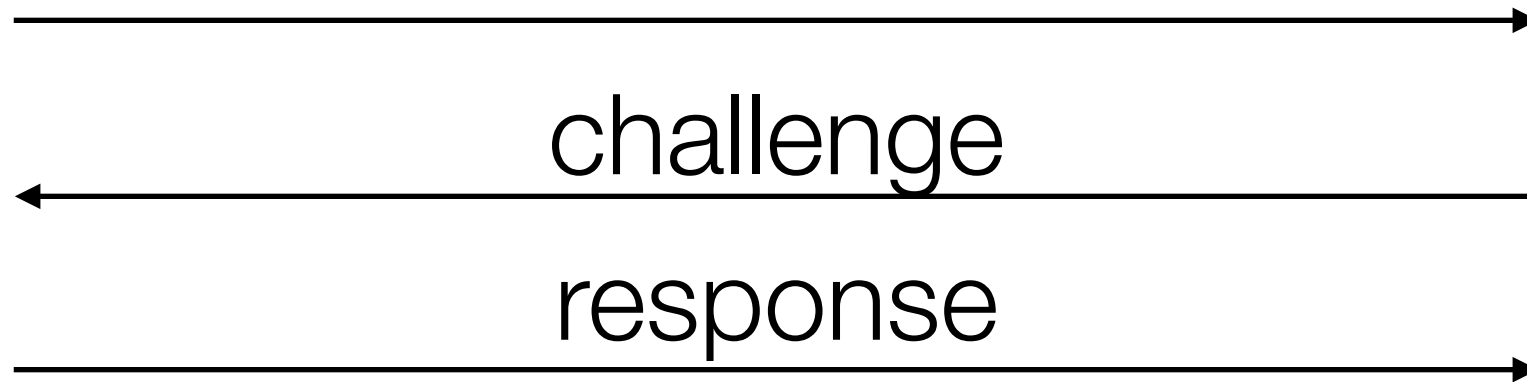
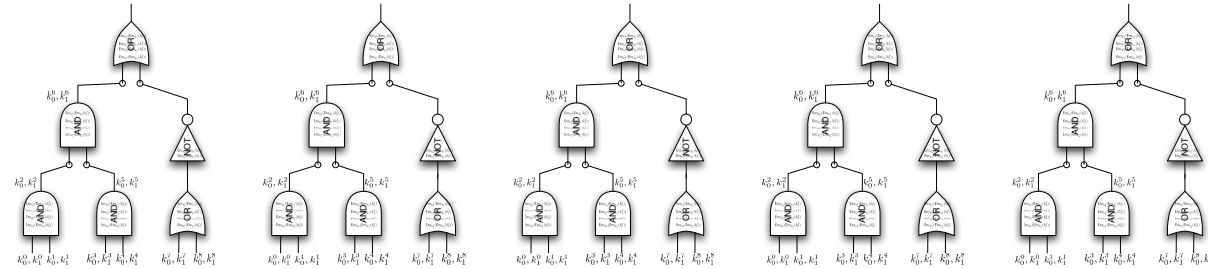


“open” challenge set of **t** circuits



random coins for challenge

Cut and Choose



Garbler sends k circuits to Evaluator.

Evaluator selects t to test.

G asks E for
random coins
used to garble.

Evaluator verifies that all t circuits are valid.

What does this
cut&choose test
accomplish?

Balls & Bins

k circuits in total



Evaluator picks c circuits to corrupt.

Garbler picks t circuits to test.

of ways to pick only good: $\binom{k-c}{t}$

of ways to pick t : $\binom{k}{t}$

Given that evaluator checks t ,
Pr that garbler succeeds in passing test:

$$\frac{\binom{k-c}{t}}{\binom{k}{t}}$$

setting $t=k/2$

Given that evaluator checks t ,
Pr that garbler succeeds in passing test:

$$\frac{\binom{k-c}{t}}{\binom{k}{t}} = \frac{(k/2)(k/2-1)\cdots(k/2-c)}{k(k-1)(k-2)\cdots(k-c)}$$

setting $t=k/2$

Given that evaluator checks t ,
Pr that garbler succeeds in passing test:

$$\frac{\binom{k-c}{t}}{\binom{k}{t}} = \frac{(k/2)(k/2-1)\cdots(k/2-c)}{k(k-1)(k-2)\cdots(k-c)} < 2^{-c}$$

setting $t=k/2$

NEGL probability that
test passes if

$O(k)$ circuits are bad

$$2^{-c} > \frac{\binom{k-c}{t}}{\binom{k}{t}} = \frac{(k/2)(k/2-1)\cdots(k/2-c)}{k(k-1)(k-2)\cdots(k-c)} \geq \left(\frac{1}{2} - \frac{c}{k}\right)^c$$

setting $t=k/2$

$$\frac{k/2-c}{k-c} \geq \frac{k/2-c}{k} \geq \left(\frac{1}{2} - \frac{c}{k}\right)$$

Noticeable probability that
 $O(1)$ circuits are corrupted

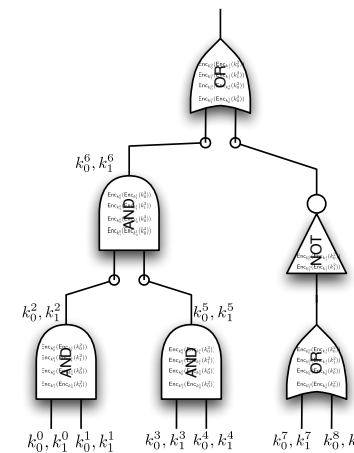
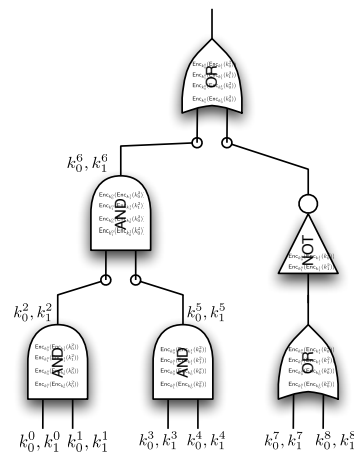
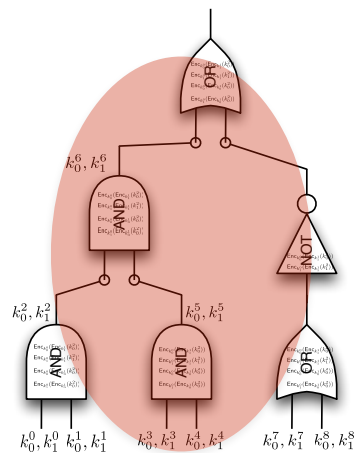
What do we do with
the remaining
circuits?

First idea:

Abort if outputs are
not all the same.

First idea:

Abort if outputs are not all the same.

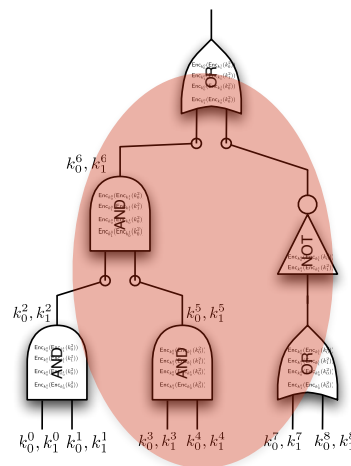


If $y_1=0$, output $f(x,y)$
else output $f(x,y)+1$

Test

$$\forall A \exists S \forall (x_1, x_2), z$$

$$\mathbf{IDEAL}_{f,S(z),I}(x_1, x_2, k) \approx_c \mathbf{REAL}_{f,A(z),I}(x_1, x_2, k)$$



If $y_1=0$, output $f(x,y)$
 else output $f(x,y)+1$

IDEAL_{S,I}



x

y

y'

abort?

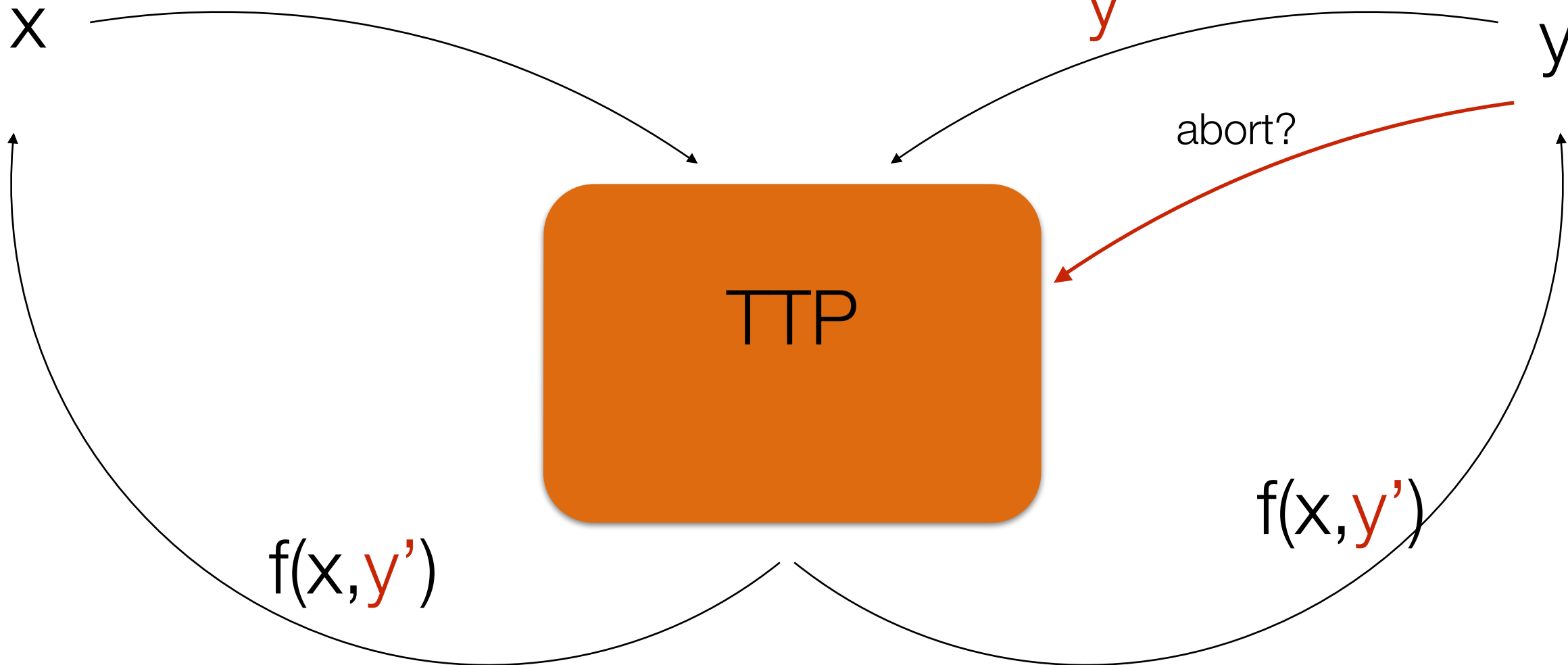
TTP

$f(x, y')$

$f(x, y')$

out: $f(x, y)$

out:?



Comment

In practice, all circuits must have same # of gates & same wiring.

Cheating restricted to changing gates.

Hard to analyze.

Second idea:

Eval all remaining circuits,
take majority output.

Third idea:

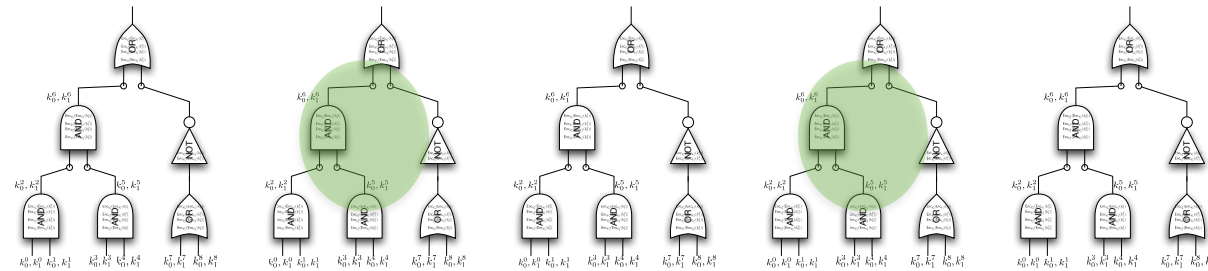
Eval all remaining circuits,
exploit cheating later.

state-of-the-art [L13]

OT



Send **k** fresh garbled circuits



challenge set of **t** circuits

random coins for challenge

majority of Eval

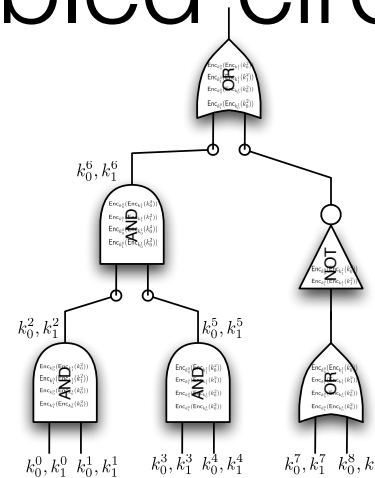
Problem: Garblers' inputs



OT



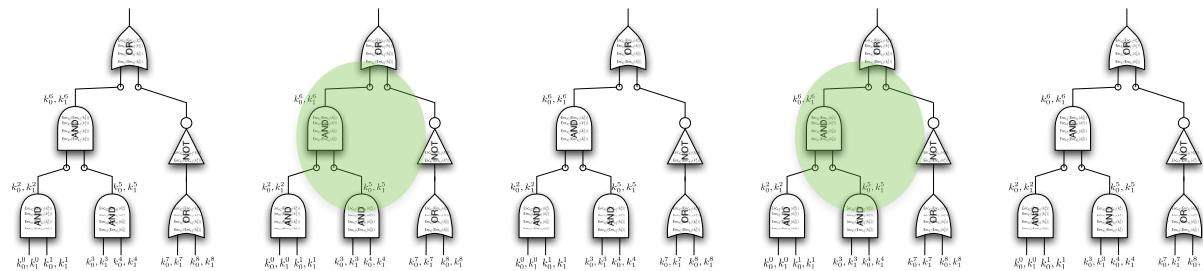
Garbled circuit



In basic protocol, garblers' input wires sent in this step.

OT

Send k fresh garbled circuits



Can't send garblers' inputs in this step anymore!

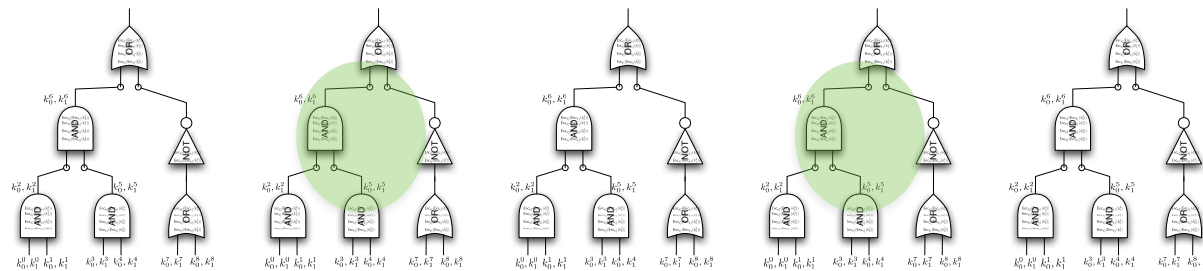
challenge set of t circuits

challenge response

majority of Eval

OT

Send k fresh garbled circuits



Can't send garblers' inputs in this step anymore!

challenge set of t circuits

challenge response

G keys

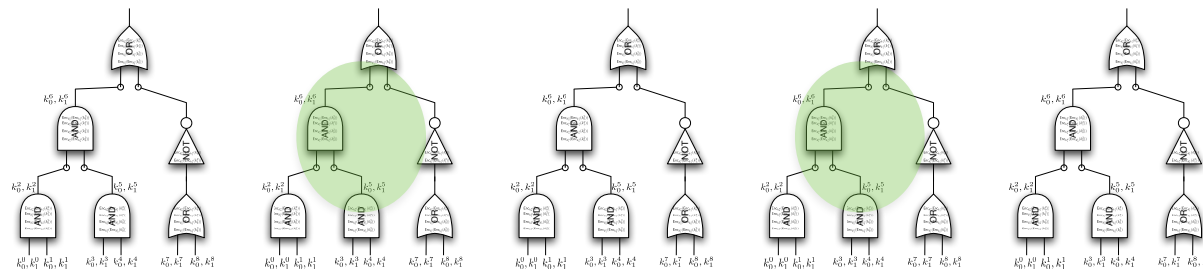
← Send here instead.

majority of Eval

Problem: Input Consistency

OT

Send **k** fresh garbled circuits



$l = k - t$ circuits
Needs all input
keys.

challenge set of **t** circuits

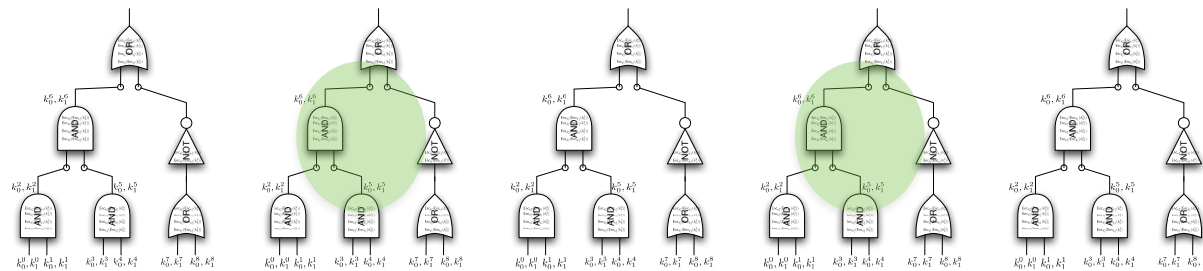
challenge response $K^1_{in}, K^2_{in}, \dots, K^l_{in}$

majority of Eval

Problem: Input Consistency

OT

Send k fresh garbled circuits



$l = k - t$ circuits
Needs all input
keys.

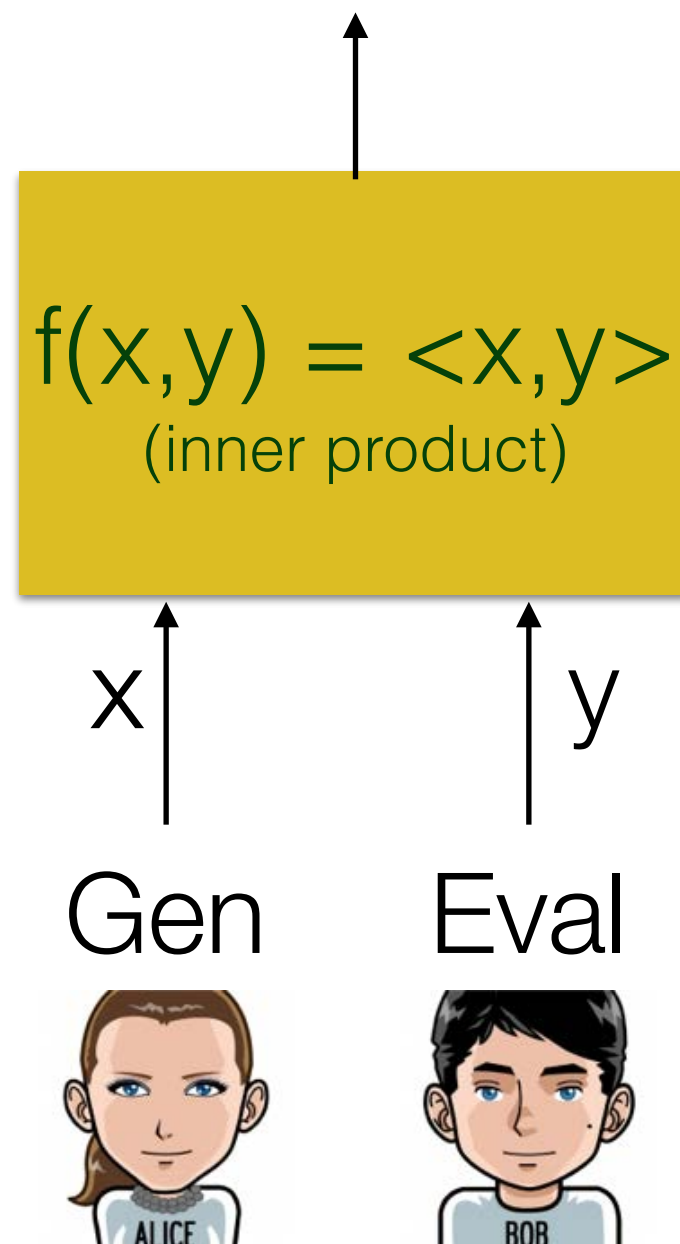
challenge set of t circuits

challenge response $K_{in}^1, K_{in}^2, \dots, K_{in}^l$

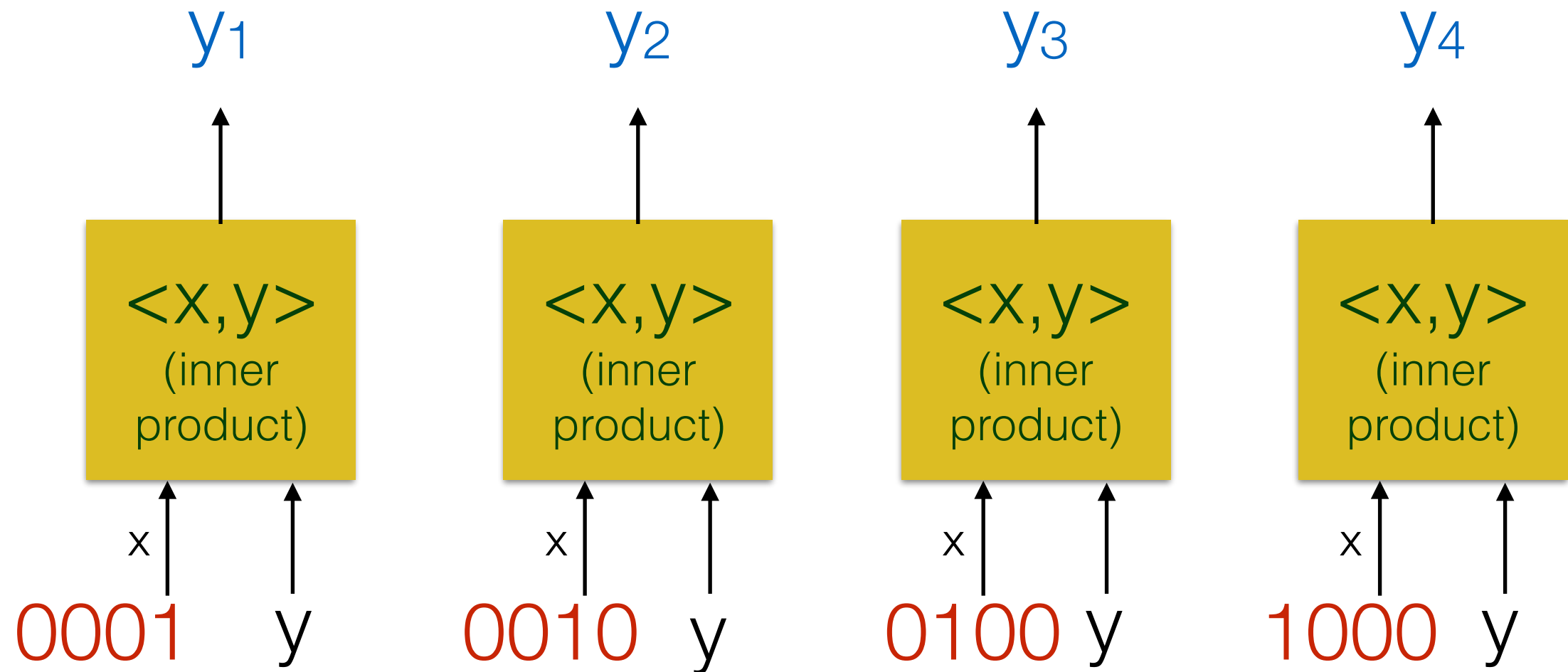
majority of Eval

What if keys do not correspond to same input?

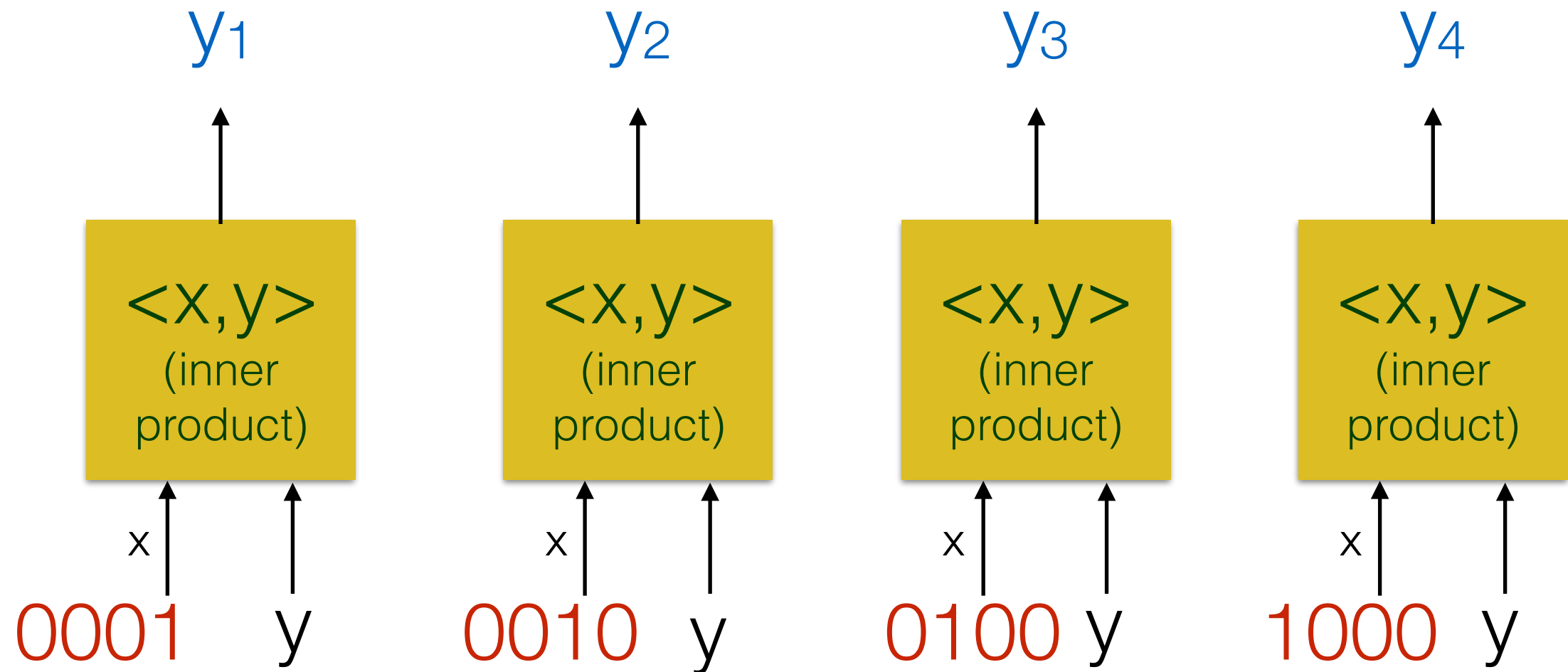
Input Consistency Attack



Input Consistency Attack



Input Consistency Attack

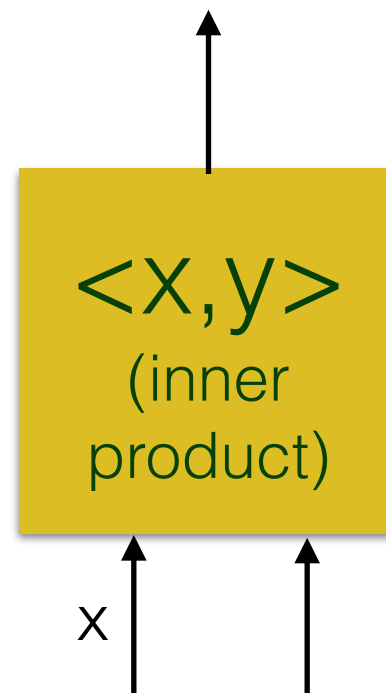


Majority(y_1, y_2, y_3, y_4)

Test

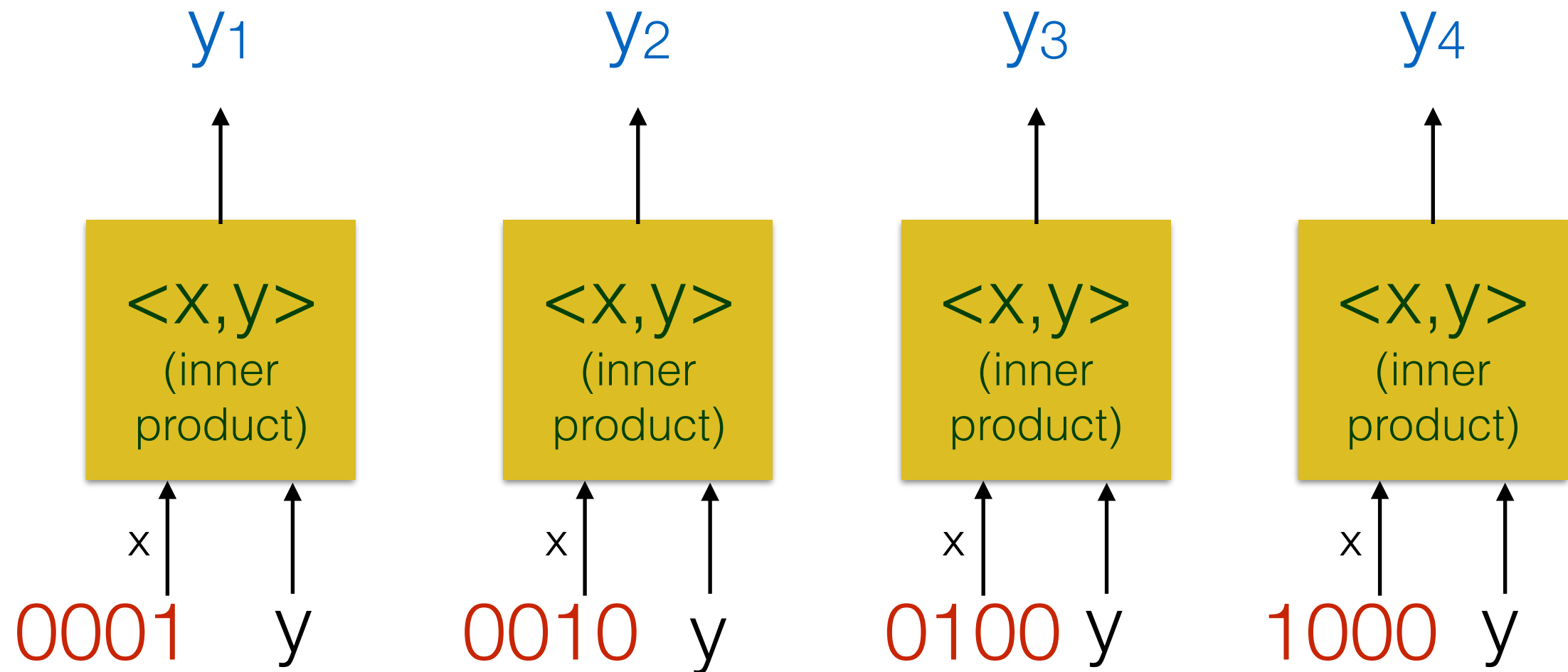
$$\forall A \exists S \forall (x_1, x_2), z$$

$$\mathbf{IDEAL}_{f,S(z),I}(x_1, x_2, k) \approx_c \mathbf{REAL}_{f,A(z),I}(x_1, x_2, k)$$



Majority(y_1, y_2, y_3, y_4)

Input Consistency Attack



Majority(y_1, y_2, y_3, y_4)

Bad!

How to handle
inconsistent inputs?

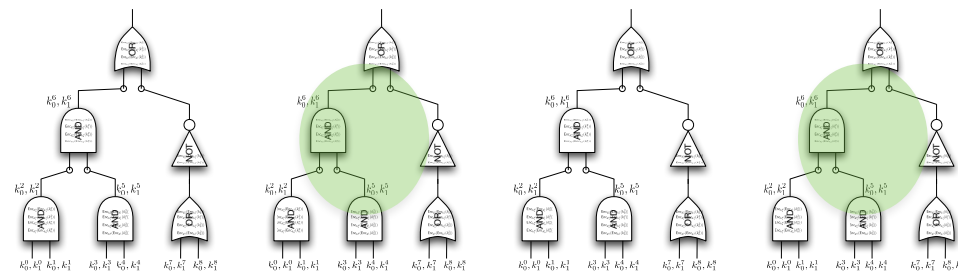
$$K^1_{\text{in}}, K^2_{\text{in}}, \dots, K^l_{\text{in}}$$

Prove consistency



OT

Send k fresh garbled circuits



π_1

challenge set of t circuits

challenge resp $K^1_{in}, \dots, K^l_{in}$ π_2

majority of Eval

Input Consistency

sym

pke

2-Outputs

sym

pke

OT +

OWF

LP07
“blackbox”

$$\Theta(k^2n)$$

$$\Theta(k^2n)$$

Kiraz08

$$\Theta(k^2n)$$

$$\Theta(kn)$$

$$\Theta(k)$$

DLOG

LP11

$$\Theta(kn)$$

$$\Theta(kn)$$

DLOG

SS11

$$\Theta(kn)$$

$$\Theta(kn)$$

$$\Theta(kn)$$

$$\Theta(kn)$$

DLOG

KSS12

“

“

“

$$\Theta(k)$$

DLOG

SS13

$$\Theta(kn)$$

$$\Theta(kn)$$

OWF

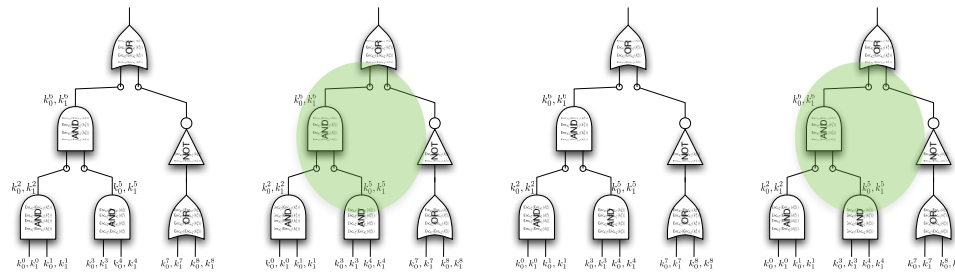
Problem: Malicious OT



Use Malic-secure OT
here. Is that enough?

OT

Send k fresh garbled circuits



π_1

challenge set of t circuits

challenge resp $K^1_{in}, \dots, K^l_{in}$ π_2

majority of Eval

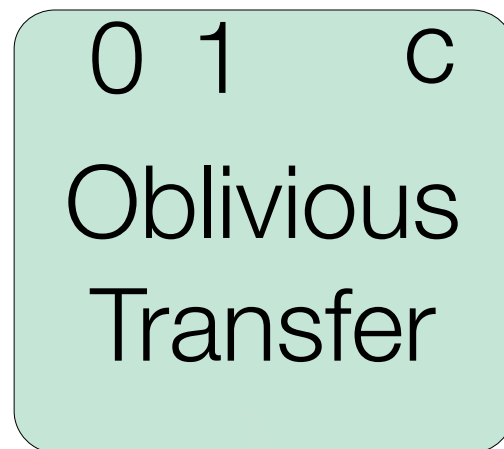


keys for $y_i=0$

$\{w_{i,0}^{(j)}\}_{j \in [k]}$

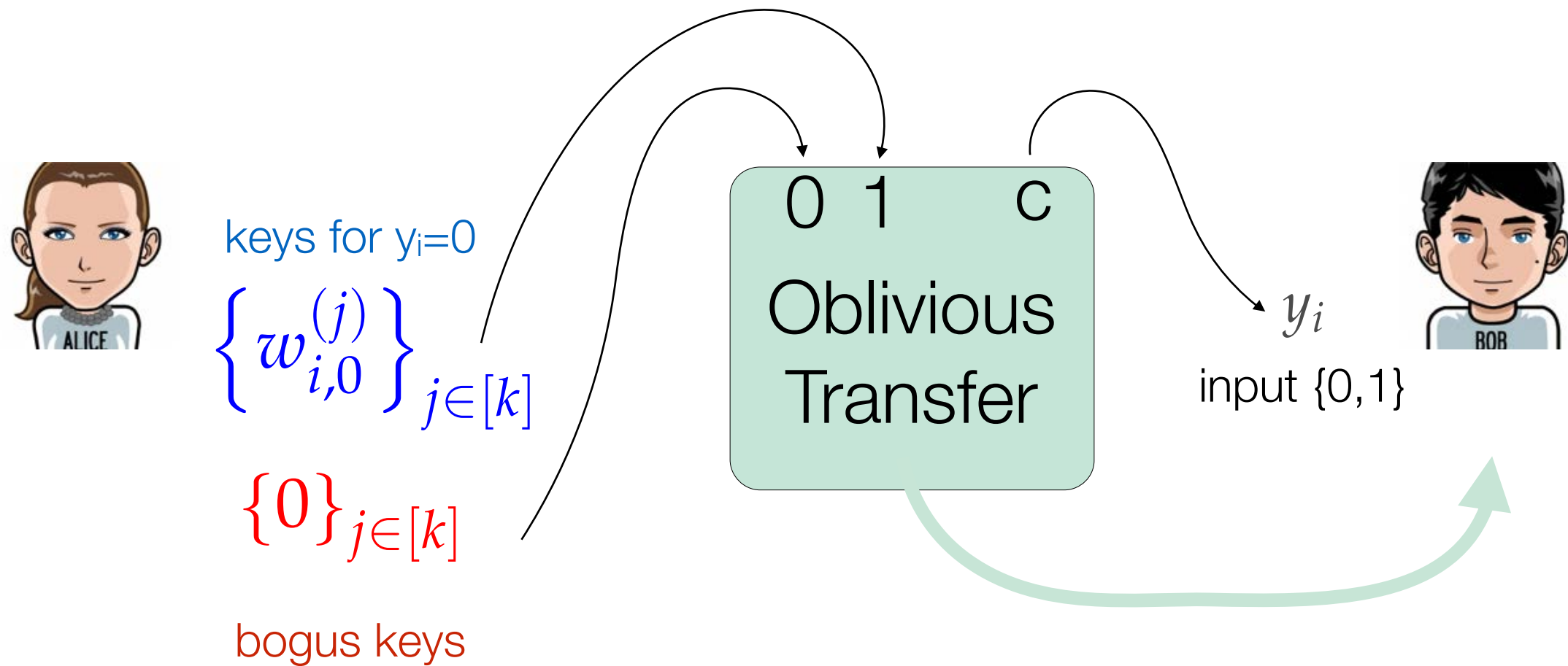
$\{w_{i,0}^{(j)}\}_{j \in [k]}$

keys for $y_i=0$



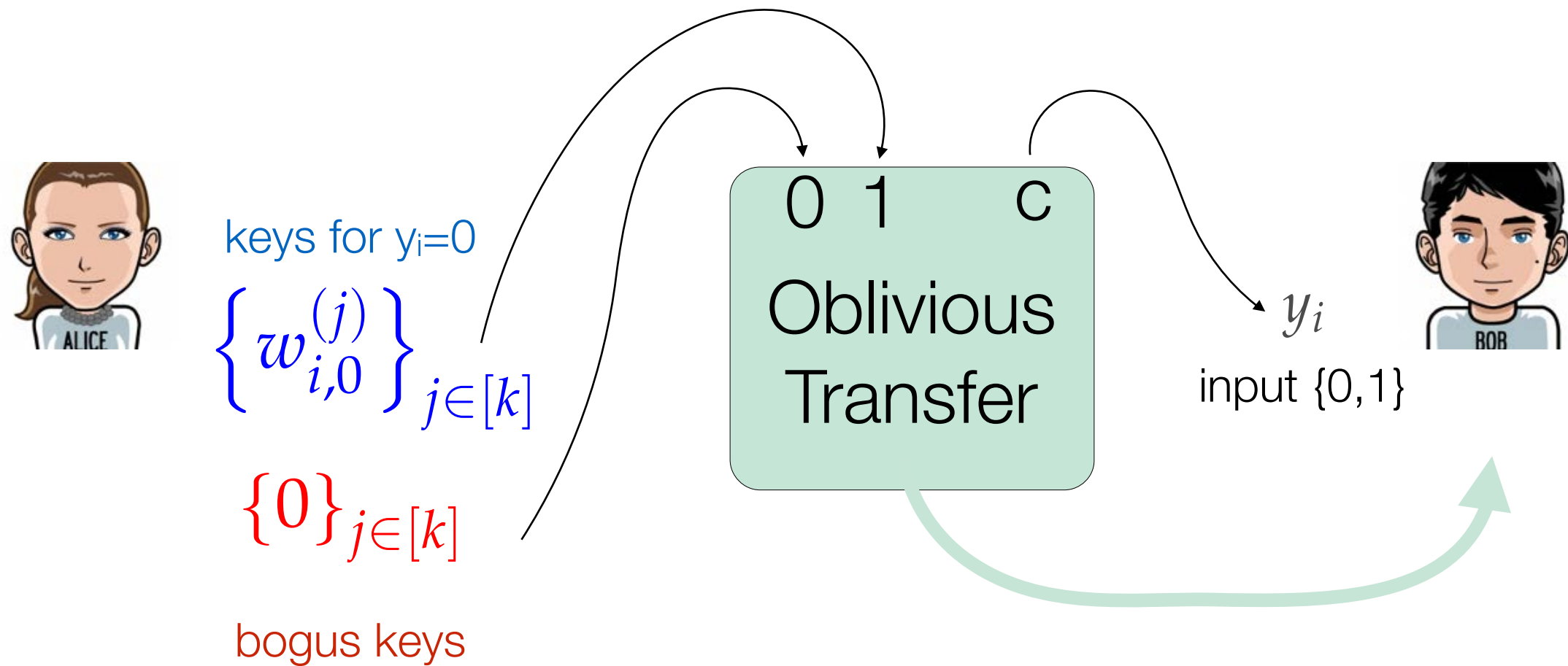
y_i
input $\{0,1\}$

Input OT
“Key management”



What are the possible outcomes?

Selective Failure attack



What are the possible outcomes?



Input $y_i = 0$

OK

Input $y_i = 1$

FAIL: Cannot Eval

Selective Failure attack

Selective Failure Solutions

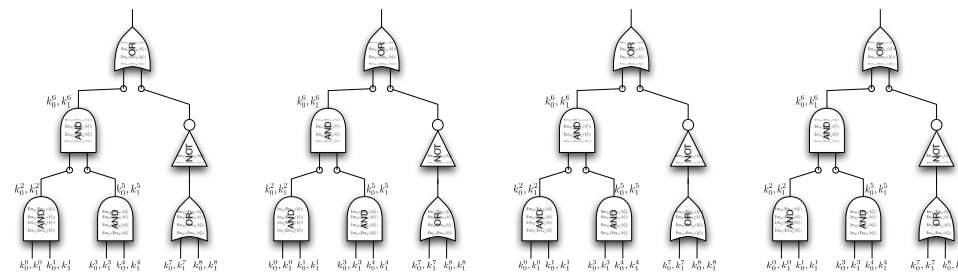
Encode inputs

Prove consistency



OT π'_1

Send k fresh garbled circuits



π_1 π'_2

challenge set of t circuits

challenge resp $K^1_{in}, \dots, K^l_{in}$ π_2

majority of Eval



Committing OT



Garbled Circuit



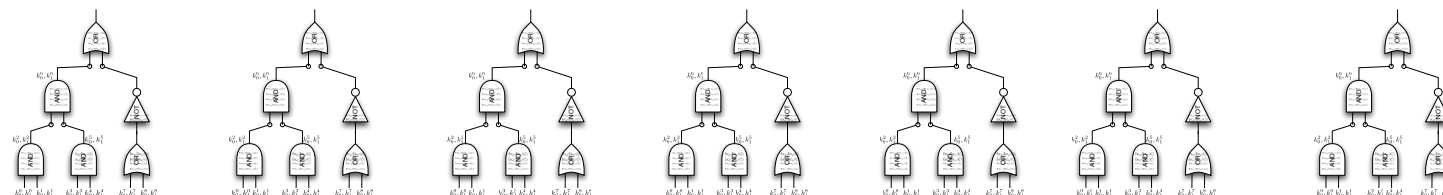
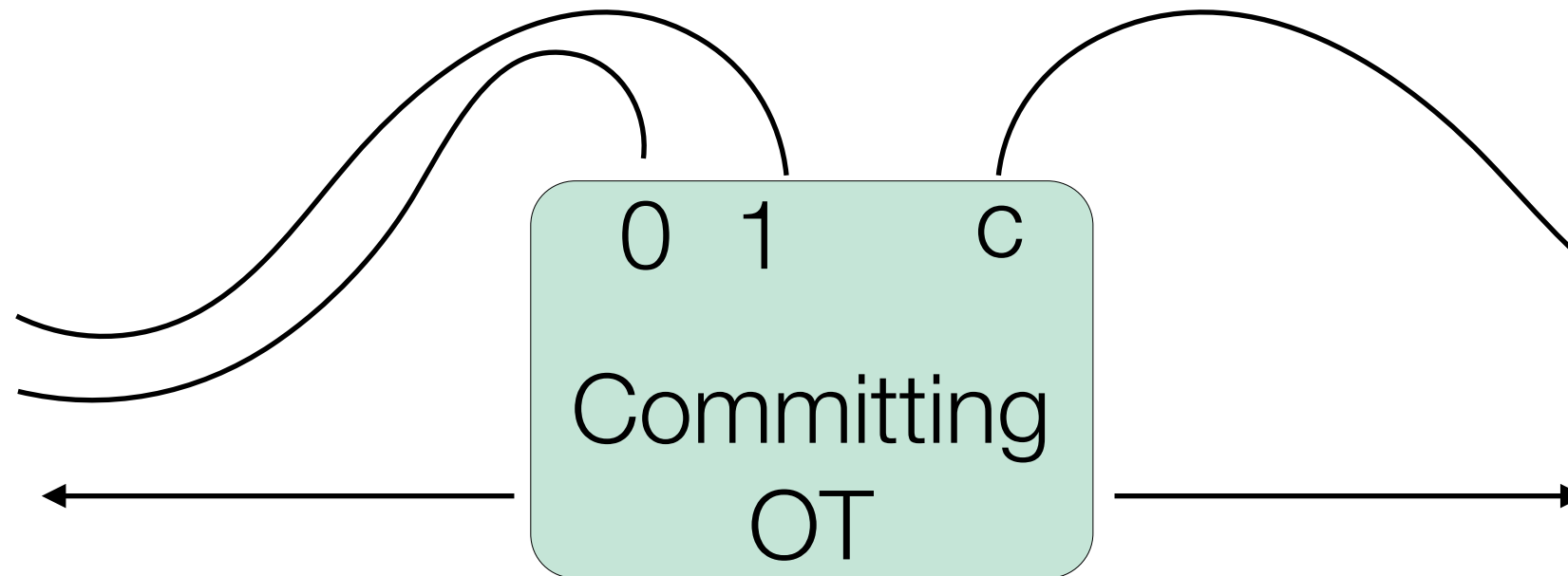
Coin flip, Cut&choose



P1 Consistency check



Circuit Eval



Com(Alice's inputs)

Coin Flipping

Open Circuits, send

Eval

Key problems for Malicious Security

Circuit Consistency

Input Consistency

Selective Failure

Output Authentication
(2-output case)

Circuit

Consistency

Given that evaluator checks t ,
Pr that garbler succeeds in passing test:

$$\frac{\binom{k-c}{t}}{\binom{k}{t}}$$

k=10. Suppose evaluator checks 1.

Garbler can choose how many to corrupt.

[illegible]

$k=10$. Suppose evaluator checks 1.

Garbler can choose how many to corrupt.

0	1	2	3	4	5	6	7	8	9	10
0	0	0	0	0	$1/2$	$2/5$	$3/10$	$1/5$	$1/10$	0

$k=10$. Suppose evaluator checks 2.

Garbler can choose how many to corrupt.

0	1	2	3	4	5	6	7	8	9	10
0	0	0	0	1/3						

$k=10$. Suppose evaluator checks 2.

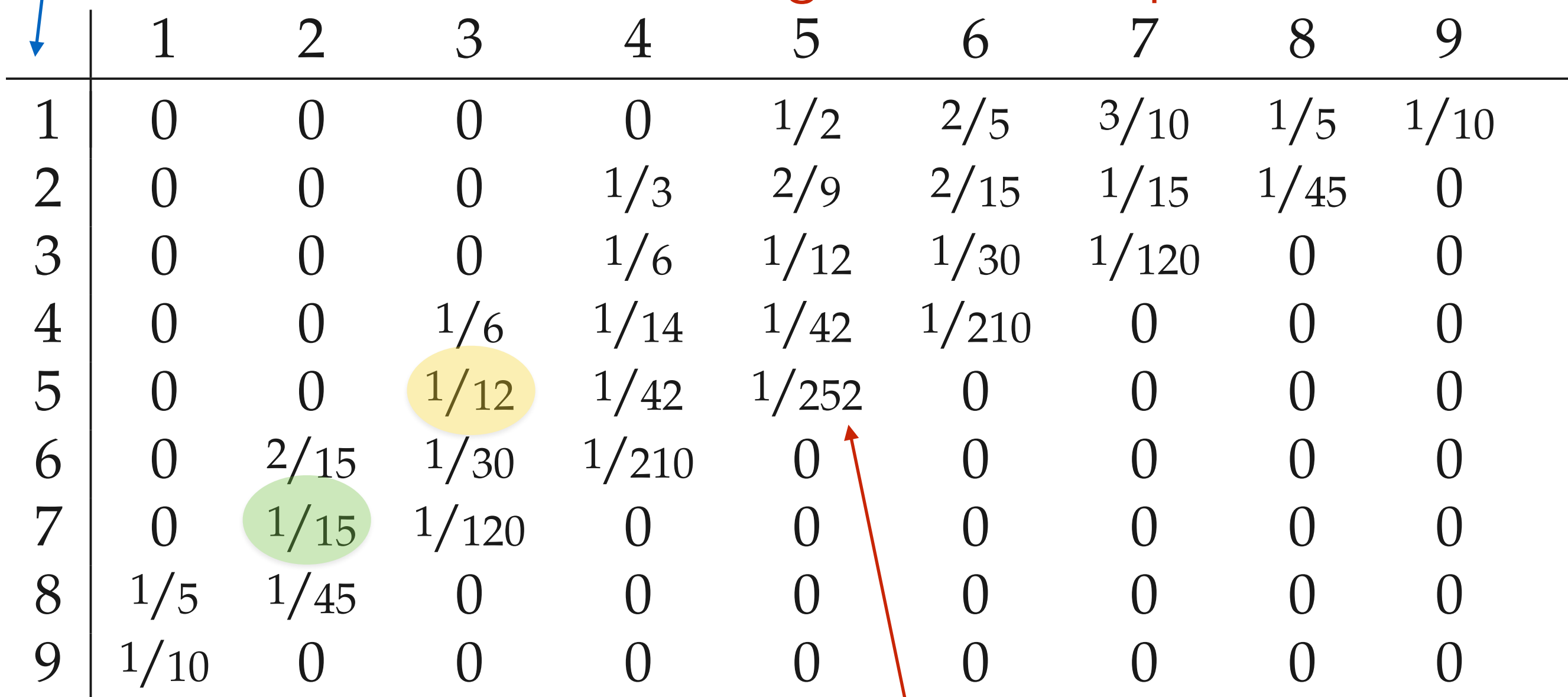
Garbler can choose how many to corrupt.

0	1	2	3	4	5	6	7	8	9	10
0	0	0	0	$1/3$	$2/9$	$2/15$	$1/15$	$1/45$	0	0

k=10

eval checks

of circuits garbler corrupts



	1	2	3	4	5	6	7	8	9
1	0	0	0	0	1/2	2/5	3/10	1/5	1/10
2	0	0	0	1/3	2/9	2/15	1/15	1/45	0
3	0	0	0	1/6	1/12	1/30	1/120	0	0
4	0	0	1/6	1/14	1/42	1/210	0	0	0
5	0	0	1/12	1/42	1/252	0	0	0	0
6	0	2/15	1/30	1/210	0	0	0	0	0
7	0	1/15	1/120	0	0	0	0	0	0
8	1/5	1/45	0	0	0	0	0	0	0
9	1/10	0	0	0	0	0	0	0	0

Pr garbler succeeds in corrupting
a majority of evaluated circuits

If eval checks t circuits,
garbler should corrupt

$$\left\lfloor \frac{(k - t) + 1}{2} \right\rfloor$$

majority of evaluated should be corrupt, no more

Evaluator should thus
check t^* circuits to
minimize

$$\min_t \left[\frac{\binom{k - \left\lfloor \frac{(k-t)+1}{2} \right\rfloor}{t}}{\binom{k}{t}} \right]$$

s copies of the circuit can yield

$$2^{-0.32s}$$

if $t^* \sim 3/5s$

Optimal for single
choice of t .

But Eval can
randomize choice of t .

Value of game

If Garbler wins, payoffs are $(1, -1)$

If Garbler loses, payoffs are $(-1, 1)$

Both parties can run probabilistic strategies.

Game is zero-sum.

min payoff that Evaluator can force =
max payoff that Garbler can achieve

We want to solve

$$\min_{e_1, \dots, e_k} \max_{x_1, \dots, x_k} \prod e_t x_c \left(\frac{\binom{k-c}{t}}{\binom{k}{t}} \right)$$

e_i : Pr that evaluator checks i

x_j : Pr that garbler corrupts j

Linear Program

Variables x_i : Pr that garbler corrupts i circuits
 $(x_1, x_2, \dots, x_n)$

Table for Eval checking 1 circuit:

0	1	2	3	4	5	6	7	8	9	10
0	0	0	0	0	$\frac{1}{2}$	$\frac{2}{5}$	$\frac{3}{10}$	$\frac{1}{5}$	$\frac{1}{10}$	0

$$v_1 = (x_1, x_2, \dots, x_n) \cdot (0, 0, 0, 0, 0, \frac{1}{2}, \frac{2}{5}, \frac{3}{10}, \frac{1}{5}, \frac{1}{10}, 0)$$

Expected payoff if Eval check 1 circuit.

$$\begin{bmatrix} 0 & 0 & 0 & 0 & 1/2 & 2/5 & 3/10 & 1/5 & 1/10 \\ 0 & 0 & 0 & 1/3 & 2/9 & 2/15 & 1/15 & 1/45 & 0 \\ 0 & 0 & 0 & 1/6 & 1/12 & 1/30 & 1/120 & 0 & 0 \\ 0 & 0 & 1/6 & 1/14 & 1/42 & 1/210 & 0 & 0 & 0 \\ 0 & 0 & 1/12 & 1/42 & 1/252 & 0 & 0 & 0 & 0 \\ 0 & 2/15 & 1/30 & 1/210 & 0 & 0 & 0 & 0 & 0 \\ 0 & 1/15 & 1/120 & 0 & 0 & 0 & 0 & 0 & 0 \\ 1/5 & 1/45 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 1/10 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \end{bmatrix} \begin{bmatrix} x_1 \\ x_2 \\ x_3 \\ x_4 \\ x_5 \\ x_6 \\ x_7 \\ x_8 \\ x_9 \end{bmatrix}$$

Evaluator chooses min row

To express as LP, add variable v.

maximize v

subject to

$$\begin{bmatrix} 0 & 0 & 0 & 0 & 1/2 & 2/5 & 3/10 & 1/5 & 1/10 & -1 \\ 0 & 0 & 0 & 1/3 & 2/9 & 2/15 & 1/15 & 1/45 & 0 & -1 \\ 0 & 0 & 0 & 1/6 & 1/12 & 1/30 & 1/120 & 0 & 0 & -1 \\ 0 & 0 & 1/6 & 1/14 & 1/42 & 1/210 & 0 & 0 & 0 & -1 \\ 0 & 0 & 1/12 & 1/42 & 1/252 & 0 & 0 & 0 & 0 & -1 \\ 0 & 2/15 & 1/30 & 1/210 & 0 & 0 & 0 & 0 & 0 & -1 \\ 0 & 1/15 & 1/120 & 0 & 0 & 0 & 0 & 0 & 0 & -1 \\ 1/5 & 1/45 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & -1 \\ 1/10 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & -1 \end{bmatrix} \begin{bmatrix} x_1 \\ x_2 \\ x_3 \\ x_4 \\ x_5 \\ x_6 \\ x_7 \\ x_8 \\ x_9 \\ v \end{bmatrix} \leq \begin{bmatrix} 0 \\ 0 \\ 0 \\ 0 \\ 0 \\ 0 \\ 0 \\ 0 \\ 0 \\ 0 \end{bmatrix}$$

$$0 \leq x_i \leq 1$$

$$\sum x_i = 1$$

```

H-representation
begin
20 11 rational
0 0 0 0 0 1/2 2/5 3/10 1/5 1/10 -1
0 0 0 0 0 1/3 2/9 2/15 1/15 1/45 0 -1
0 0 0 0 0 1/6 1/12 1/30 1/120 0 0 -1
0 0 0 1/6 1/14 1/42 1/210 0 0 0 -1
0 0 0 1/12 1/42 1/252 0 0 0 0 -1
0 0 2/15 1/30 1/210 0 0 0 0 0 -1
0 0 1/15 1/120 0 0 0 0 0 0 -1
0 1/5 1/45 0 0 0 0 0 0 0 -1
0 1/10 0 0 0 0 0 0 0 0 -1
1 -1 -1 -1 -1 -1 -1 -1 -1 -1 0
-1 1 1 1 1 1 1 1 1 1 0
0 1 0 0 0 0 0 0 0 0 0
0 0 1 0 0 0 0 0 0 0 0
0 0 0 1 0 0 0 0 0 0 0
0 0 0 0 1 0 0 0 0 0 0
0 0 0 0 0 1 0 0 0 0 0
0 0 0 0 0 0 1 0 0 0 0
0 0 0 0 0 0 0 1 0 0 0
0 0 0 0 0 0 0 0 1 0 0
end
maximize
0 0 0 0 0 0 0 0 0 0 1

```

```

*cdd+: Double Description Method in C++:Version 0.77(August 19, 2003)
* Copyright (C) 1999, Komei Fukuda, fukuda@ifor.math.ethz.ch
* Compiled for Rational Exact Arithmetic with GMP
*cdd LP Result
*cdd input file : 10.in (20 x 11)
*LP solver: Dual Simplex
*LP status: a dual pair (x, y) of optimal solutions found.
*maximization is chosen.
*Objective function is
  0 + 0 X[1] + 0 X[2] + 0 X[3] + 0 X[4] +
  0 X[5] + 0 X[6] + 0 X[7] + 0 X[8] + 0 X[9] +
  1 X[10]
*LP status: a dual pair (x, y) of optimal solutions found.
begin
  primal_solution
  1 : 60/247
  2 : 575/1729
  3 : 440/1729
  4 : 30/247
  5 : 12/247
  6 : 0
  7 : 0
  8 : 0
  9 : 0
  10 : 6/247
  dual_solution
  19 : 23/1235
  20 : 53/2470
  17 : 23/2470
  18 : 147/9880
  1 : 7/247
  3 : 27/247
  5 : 63/247
  7 : 90/247
  9 : 60/247
  10 : 6/247
  optimal_value : 6/247
end
*number of pivot operations = 5
*Computation starts at Sun Feb 15 06:50:05 2015
*
* terminates at Sun Feb 15 06:50:05 2015
*Total processor time = 0 seconds
*
* = 0h 0m 0s

```

6/247 ~ .02429

2^{-5.3}

60/247 575/1729 440/1729 30/247 12/247

		1	2	3	4	5	6	7	8	9
$7/247$	1	0	0	0	0	$1/2$	$2/5$	$3/10$	$1/5$	$1/10$
	2	0	0	0	$1/3$	$2/9$	$2/15$	$1/15$	$1/45$	0
$27/247$	3	0	0	0	$1/6$	$1/12$	$1/30$	$1/120$	0	0
	4	0	0	$1/6$	$1/14$	$1/42$	$1/210$	0	0	0
$63/247$	5	0	0	$1/12$	$1/42$	$1/252$	0	0	0	0
	6	0	$2/15$	$1/30$	$1/210$	0	0	0	0	0
$90/247$	7	0	$1/15$	$1/120$	0	0	0	0	0	0
	8	$1/5$	$1/45$	0	0	0	0	0	0	0
$60/247$	9	$1/10$	0	0	0	0	0	0	0	0

Solution for k=10

k=41

primal_solution

1 : 10645508192981161500/20055554759628164776001
2 : 311397613586611188434870/96407051729532588078236807
3 : 1160462119873878916970070/96407051729532588078236807
4 : 161244094440834884924757/5074055354185925688328253
5 : 325255554436935813832401/5074055354185925688328253
6 : 95452384789288218166605/922555518942895579696046
7 : 1398734699891587882768035/10148110708371851376656506
8 : 786108086596520648697555/5074055354185925688328253
9 : 68900733695195588092725/461277759471447789848023
10 : 57701938641754468976460/461277759471447789848023
11 : 42391924836751780371900/461277759471447789848023
12 : 27537371265736096865100/461277759471447789848023
13 : 15916990323524614014600/461277759471447789848023
14 : 8228586854967489164700/461277759471447789848023
15 : 3820473545668824762900/461277759471447789848023
16 : 1598383883392727312700/461277759471447789848023
17 : 604090345871550037500/461277759471447789848023
18 : 206458340712361920000/461277759471447789848023
19 : 2765067063111990000/20055554759628164776001
20 : 1013857923141063000/20055554759628164776001
21 : 0
22 : 0
23 : 0
24 : 0
25 : 0
26 : 0
27 : 0
28 : 0
29 : 0
30 : 0
31 : 0
32 : 0
33 : 0
34 : 0
35 : 0
36 : 0
37 : 0
38 : 0
39 : 0
40 : 0
41 : 10645508192981161500/822277745144754755816041

dual_solution

2-16.2

k=117 .0000000000000034624553 $2^{-41.3}$

versus

k=125 in SS11